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Efficient reconfigurable parallel switching for low-density parity-check encoding and decoding

Divyashree Yamadur Venkatesh[1], Komala Mallikarjunaiah[1], Mallikarjunaswamy Srikantaswamy[2]
[1]Department of Electronics and Communication Engineering, SJB Institute of Technology, Bengaluru, India
[2]Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Bengaluru, India

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ABSTRACT

In the evolution of next-generation communication systems, the demand for higher data integrity and transmission efficiency has brought low-density parity-check (LDPC) codes into focus, particularly for their error-correcting prowess. Traditional LDPC encoding and decoding techniques, such as the belief propagation (BP), Min-Sum, and Sum-Product algorithms, are hampered by high computational complexity and latency. Our research introduces a groundbreaking approach: an efficient, reconfigurable high-speed parallel switching operation for a complexity-optimized low-density parity-check encoding and decoding model (CoLDPC-EC). This method leverages advanced parallel processing and reconfigurable computing to drastically enhance operational speed and efficiency. It significantly outperforms conventional algorithms by optimizing key parameters like decoding throughput and power consumption, ensuring swift, energy-efficient error correction ideal for cutting-edge communication technologies. Our comparison with traditional methods underscores our solution's superior speed, flexibility, and efficiency, promising a leap forward in reliable, high-speed data transmission for next-generation networks. As per the simulation analysis, the proposed system shows better performance compared to conventional methods by 10.35%, 3.56%, and 2.36% in terms of decoding throughput, power consumption, and energy efficiency error correction, respectively.

Corresponding Author:

Mallikarjunaswamy Srikantaswamy
Department of Electronics and Communication Engineering, JSS Science and Technology University
Bengaluru 560060, India
Email: pruthvi.malli@gmail.com

1. INTRODUCTION

In the quest for achieving unparalleled efficiency and reliability in next-generation communication systems, the focus on advanced error-correcting codes, specifically low-density parity-check (LDPC) codes, has intensified [1]. LDPC codes, known for their remarkable ability to approach the Shannon limit, are crucial in enhancing the quality and reliability of data transmission across various communication channels. However, as the volume of data and the speed of transmission continue to escalate, traditional LDPC encoding and decoding methods struggle to meet the increasing demands for high-speed processing and energy efficiency. This challenge has spurred interest in high-speed parallel switching operations for LDPC encoding and decoding, a promising avenue for mitigating the limitations of conventional approaches [2]. Figure 1 shows the intricate process of encoding and decoding data in a communication system using LDPC codes. Initially, a transport block (TB) cyclic redundancy check (CRC) is applied to the data to detect any errors that might occur during transmission. The base graph (BG) selection stage follows, determining the structure of the LDPC

encoder's parity-check matrix. After this, code block (CB) segmentation divides the data into smaller blocks, which are then encoded using LDPC codes in the LDPC encoding step, introducing redundancy to enable error correction. Subsequently, the rate matching procedure adjusts the rate of the encoded blocks to fit the channel's bandwidth constraints, either by adding or puncturing bits [3], [4]. The CB concatenation phase consolidates these blocks into a single stream for transmission, which is then modulated into an analog signal suited for the communication channel. After traversing the channel, the signal is demodulated back into a digital format. CB deconcatenation separates the stream into individual blocks, and rate dematching restores the original data rate. LDPC decoding removes redundancy and corrects errors within the blocks. A CRC follows to ensure the integrity of the decoded data. Finally, error calculation assesses the performance of the communication system by determining the final error metrics of the transmission. Each step is essential for maintaining the reliability and effectiveness of data communication, with LDPC codes significantly enhancing error correction capabilities [5].

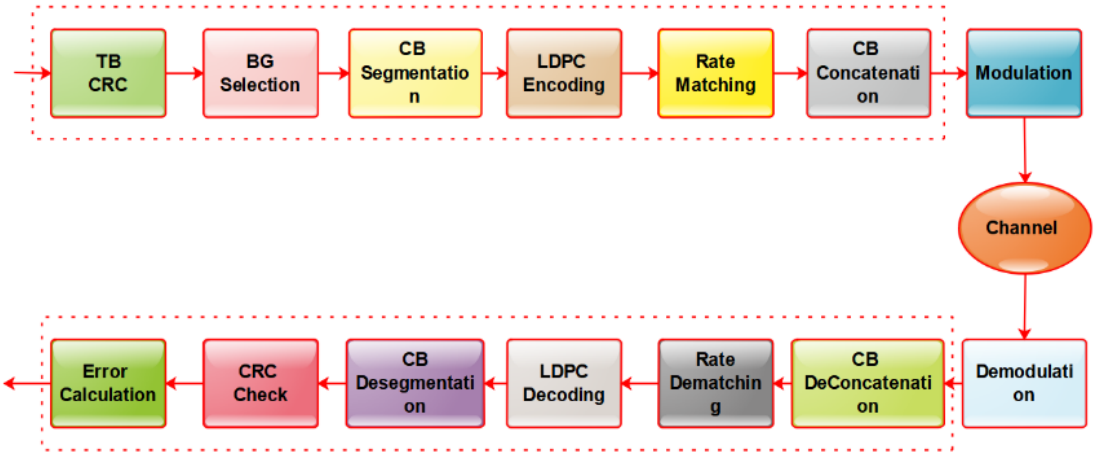

Figure 1. The fundamental structure of an LDPC encoder and decoder for a communication system

Recent trends in communication technology, such as the deployment of 5G networks and beyond, internet of things (IoT) ecosystems, and deep-space communication, underscore the need for robust and efficient error-correcting mechanisms [6]. These applications demand not only high data integrity but also the ability to process information rapidly and energy-efficiently. In this context, parallel processing emerges as a key strategy, offering a pathway to significantly accelerate LDPC code operations while minimizing power consumption. Despite these advancements, there remains a notable research gap in fully harnessing parallel computing technologies for LDPC encoding and decoding. Specifically, existing solutions often exhibit scalability limitations and struggle to adapt to the dynamic requirements of modern communication systems, highlighting the need for more flexible and efficient methodologies [7].

The application of high-speed parallel switching operations in LDPC encoding and decoding extends across several critical areas of modern communication. For instance, in satellite communications, where the reliability of data transmission is paramount, these methods can drastically improve error correction without compromising on speed or consuming excessive power [8]. Similarly, in high-speed broadband networks, enhancing the efficiency of LDPC encoding and decoding can significantly boost the overall system performance, catering to the ever-growing demand for faster internet services. Furthermore, in the burgeoning field of wireless sensor networks, which are integral to IoT applications, the adoption of these advanced techniques could resolve existing bottlenecks in data reliability and processing speed, paving the way for more seamless and efficient IoT deployments. Collectively, these applications highlight the broad potential and urgent need for innovative approaches in LDPC encoding and decoding, underscoring the importance of this research in shaping the future of communication technologies [9].

2. RELATED WORKS

In the sphere of LDPC encoding and decoding for next-generation communication systems, numerous researchers have contributed valuable insights and advancements. Chen *et al.* [10] proposed a novel reconfigurable computing approach for LDPC decoding, aiming to enhance flexibility and adaptability in various communication scenarios. Their method showed promise in terms of reconfigurability and energy

efficiency, yet it lacked in providing a comprehensive solution to reduce latency significantly. On another front, Nakamura *et al*. [11] focused on harnessing graphics processing unit (GPU)-based parallel processing for LDPC decoding, which led to substantial gains in decoding throughput. However, their technique was constrained by the inherent limitations of GPU architectures, including memory bandwidth and synchronization issues.

Recently, Song *et al*. [12] embarked on integrating machine learning techniques with LDPC decoding to dynamically adjust the decoding process based on the channel conditions. This approach marked a significant step towards intelligent error correction systems, offering adaptability and improved performance. Nevertheless, the dependency on extensive training datasets and potential overfitting to specific channel models emerged as areas needing further exploration [13]. These studies collectively underscore the ongoing efforts to refine LDPC encoding and decoding for enhanced performance in communication systems. Each work contributes to the understanding of potential improvements while also revealing the multifaceted challenges that remain, such as achieving the ideal balance between computational efficiency, scalability, and adaptability in diverse communication environments [14].

3. METHODOLOGY

Figure 2 shows the flow of data through the proposed complexity-optimized low-density parity-check encoding and decoding model (CoLDPC-EC) system. It starts with raw data input, followed by several processing stages, including error checking, segmentation, encoding, rate matching, modulation, transmission, demodulation, rate dematching, decoding, de-concatenation, and final error checking, before outputting the processed data. Each stage is crucial in ensuring the reliability and efficiency of the communication system [15]–[17]. The model also includes dynamic adjustments and reconfiguration mechanisms to optimize performance based on real-time conditions. This involves dynamically changing the density or structure of the parity-check matrix, adjusting the number of iterations in decoding based on error rates, and utilizing probabilistic message passing and dynamic check node processing to enhance error correction capabilities [18]–[20].

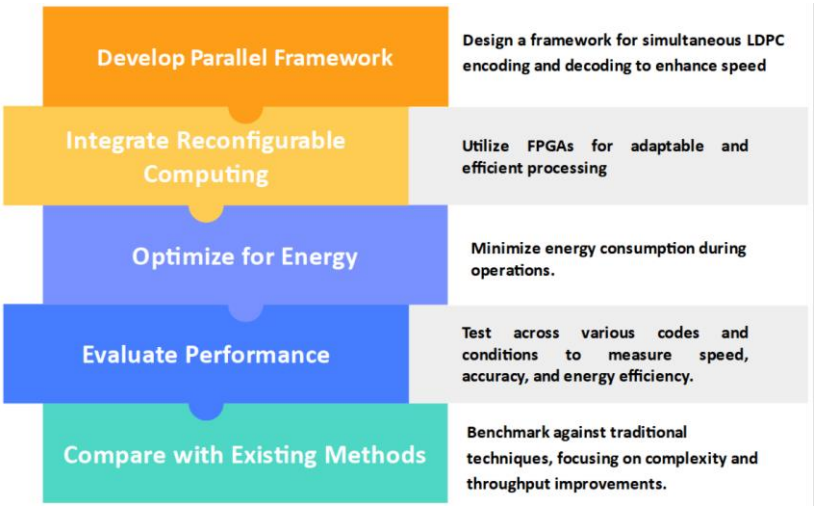

Figure 2. Proposed methodology for CoLDPC-EC

4. PROPOSED CoLDPC-EC

The Figure 3 shows the process of proposed CoLDPC-EC model, designed to ensure reliable transmission with error correction capabilities. The process begins at the data input interface, where the raw data is initially introduced into the system. Here, the data undergoes a TB CRC to detect any corruption or errors that may have occurred before it enters the encoding phase. This check acts as an early safeguard to ensure data integrity. Once cleared, the BG selection takes place, which involves choosing an appropriate LDPC code structure [21]. This selection is critical as it determines the efficiency and complexity of the encoding process. The data moves into CB segmentation, where it is divided into smaller, more manageable segments. These segments are then fed into parallel LDPC encoders [22]. The parallel processing allows for multiple data blocks to be encoded simultaneously, significantly speeding up the operation. The encoded data

is then passed through the switching fabric, a dynamic routing mechanism that efficiently directs the data to the correct transmission channels or subsequent stages. The rate matching step follows, where the encoded data is adjusted to suit the transmission channel's bandwidth, either by adding or omitting bits. The appropriately rate-matched data is then modulated for transmission across the channel, which can be any physical or wireless medium. Upon reaching the receiving end, the signal is demodulated back into a digital format. The rate dematching process then reconstructs the data stream to its original rate, compensating for the earlier rate matching adjustments. Once demodulated, the data is passed through parallel LDPC decoders that work in unison to decode the multiple data streams, utilizing the redundancy added earlier to correct any errors. The CB deconcatenation step reassembles the decoded data blocks into their original sequence [23]–[25]. A final CRC verification is performed to ensure the data's integrity post-decoding. The process concludes at the data output interface, where the decoded and verified data is outputted, ready for use or further processing.

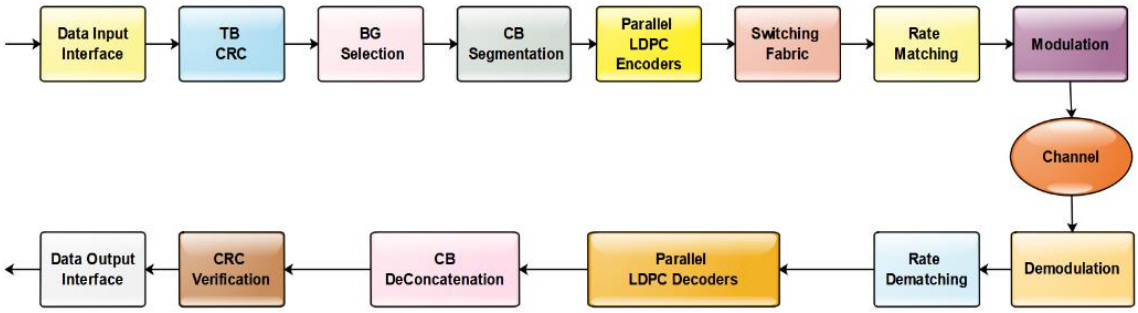

Figure 3. The proposed CoLDPC-EC for next generation communication system

5. PROPOSED MATHEMATICAL MODEL

The proposed mathematical model for the CoLDPC-EC system involves creating parallel algorithms that can dynamically adjust to varying encoding and decoding complexities as well as changing channel conditions. This model ensures minimal latency, optimal throughput, and adaptability across different data rates and sizes. The system is designed to handle real-time data with high performance and reliability, making it suitable for next-generation communication systems. By leveraging parallel processing, the model optimizes the use of computational resources, ensuring efficient data transmission with minimal delays, even in high-noise environments or when dealing with large volumes of data.

5.1. Mathematical model for parallel low-density parity-check encoding

A mathematical model specifically for parallel LDPC encoding, we can focus on a distributed approach that allows for encoding across multiple processors or cores. The model should efficiently utilize multiple processors to encode large amounts of data simultaneously, ensuring both speed and accuracy. The mathematical model for parallel LDPC encoding leverages a distributed approach to enhance efficiency and speed. By using a sparse parity-check matrix H, the encoding process adapts dynamically to channel conditions, allowing multiple data blocks to be processed simultaneously by different processors. This method significantly reduces encoding time while maintaining accuracy, ensuring optimal performance in high-speed data transmission environments.

5.2. Sparse parity-check matrix adaptation

Let H represent the sparse binary $m \times n$ parity-check matrix. The matrix can dynamically change its density or structure for complexity optimization based on the channel conditions and system requirements and (1) shows the parity check matrix adaptation. Where F_{adapt} is the adaptation function, and C is the set of channel conditions or system requirements.

$$H_{config} = F_{adapt}(H, C) \quad (1)$$

5.3. Parallel encoding structure

In a parallel encoding structure for LDPC codes, the data is divided into blocks that are processed simultaneously by multiple encoders. Each encoder operates on its block independently, significantly reducing the overall encoding time. This method leverages the power of concurrency, exploiting the sparse nature of

LDPC matrices to optimize encoding operations across different processors and the message partition is given in (2) and encode segment in parallel process is represented in (3).

Partition the message vector u into p segments, $u = [u_1, u_2, \dots, u_p]$ (2)

Encode segments in parallel: $c_i = u_i G_i$ (3)

where G_i corresponds to the submatrix of G.

5.4. Switching fabric for encoding

The switching fabric in the context of encoding acts as a dynamic router, directing encoded data blocks from parallel LDPC encoders to their subsequent processing stages or output channels. It efficiently manages the flow of data within the system, ensuring optimal utilization of resources and maintaining the integrity of the encoded sequences as they converge from the distributed encoding units. Define a switching operation S_e that routes the encoded segments c_i to the appropriate channels or processors and the switching fabric encoder is given in (4).

$$v' = S_e(c_1, c_2, \dots, c_p) \quad (4)$$

Ensuring that the switching fabric reconfigures based on the current encoding task requirements.

5.5. Mathematical model for parallel low-density parity-check decoding

The parallel LDPC decoding model leverages multiple processors to decode different segments of a codeword simultaneously, significantly speeding up the error correction process. By distributing the computational workload and synchronizing message updates across the system, the model enhances overall decoding efficiency, reducing latency, and improving error-correction performance in high-speed communication systems. This parallel processing approach ensures that larger and more complex codewords can be decoded in real time, making it highly suitable for next-generation data transmission requirements.

5.6. Probabilistic message passing

Probabilistic message passing for LDPC decoding involves iteratively updating and exchanging likelihood estimates between nodes in a graph to correct errors in transmitted data. This method leverages probabilities to infer the most likely original message, enhancing decoding accuracy and efficiency. The probabilistic message passing for decoding with log likelihood ratio (LLR) calculation has been done by (5).

$$L(r_i) = log \frac{(P(r_i \mid c_i=1)}{P(r_i \mid c_i=0)} \quad (5)$$

The (6) shows the update LLRs in parallel with a high-speed operation.

$$L(l+1)(c_i) = L(r_i) + \sum_{c \in N(i)} M_{c \to i}^{(l)} \quad (6)$$

5.7. Dynamic check node processing

Dynamic check node processing allocates computational resources adaptively during LDPC decoding, adjusting to the varying complexity of different check nodes. This strategy optimizes the decoding process by focusing on nodes requiring more intensive computation, ensuring efficient error correction. The dynamically allocate check node processors based on the check node degrees and system load. The (7) represented check nodes update messages in parallel.

$$M_{c \to v}^{(l+1)} = f_{check}\,(M_{c \to v}^{(l)}, H_{config}) \quad (7)$$

Where f_{check} being the check node update function optimized for parallel execution, is the message sent from check node c to variable node v in the $(l+1)th$ iteration of LDPC code decoding, indicating the probability of a bit's value based on surrounding check, $M_{c \to v}^{(l)}$, represents the message from check node c to variable node v at iteration l in LDPC decoding, conveying information about the likelihood of a bit's value

5.8. Switching fabric for decoding

The switching operation S_d for the decoding phase dynamically routes messages between variable and check nodes. The operation optimizes the message flow based on decoding iterations and error patterns as given in (8).

$$Sd(\{M_{c\to v}^{(l)}\},\{M_{v\to c}^{(l)}) \quad (8)$$

5.9. Reconfigurable iterative decoding

Reconfigurable iterative decoding utilizes an adaptive algorithm that adjusts the number of iterations based on observed error rates and convergence patterns. This approach ensures efficient error correction by dynamically configuring the decoding process to terminate when optimal conditions are met, thereby reducing latency and improving throughput in next-generation communication systems.Implement an iterative decoding algorithm that can reconfigure the number of iterations based on the observed error rate and convergence patterns. Terminate decoding based on a decision algorithm D that evaluates the condition $Hc\hat{}T$=0 or a maximum number of iterations.

5.10. System-level optimization

System-level optimization for LDPC decoding strategically allocates computational resources and adjusts decoding parameters in real-time, enabling enhanced efficiency and throughput. By dynamically adapting to varying data rates and changing channel conditions, this approach ensures optimal use of processing power, minimizing delays, and maximizing error-correction performance. The real-time adjustments improve the overall system's reliability and performance, especially in high-speed communication networks where rapid and accurate data transmission is essential. This optimization is key for maintaining high-performance standards in next-generation communication systems.

5.11. Complexity optimization

Complexity optimization involves balancing decoding performance with computational resource utilization. The optimization function dynamically adjusts the parity-check matrix, data partitioning, and parallel processing structures to minimize complexity while maximizing efficiency, enabling robust, and scalable LDPC encoding and decoding operations. The complexity optimization function $O(\cdot)$ balances the trade-off between the decoding performance and the computational resources. This function dynamically adjusts H_{config}, the partitioning of u, and the parallelism in S_e and S_d.

5.12. High-speed operation

High-speed operation in LDPC encoding and decoding is achieved through streamlined processes and advanced parallel processing techniques. The system leverages high-speed switching fabrics and dynamic reconfiguration to handle large data rates and ensure rapid, reliable data transmission, essential for next-generation communication technologies. Ensure that the entire encoding and decoding process is streamlined for high-speed data processing, particularly within the switching fabric operations.

5.13. Reconfigurability for adaptation

The model integrates a reconfigurability mechanism $R(\cdot)$ that allows the system to adapt to changing conditions in real-time, optimizing the switching fabric and the parallelism for current encoding and decoding tasks. This model leverages dynamic reconfiguration and high-speed parallel processing to adapt to varying complexities and conditions, aiming for robust performance in next-generation communication systems. Each component from the LDPC encoder and decoder to the switching fabric must be optimized to work cohesively, ensuring that the system can handle high data rates and maintain.

6. RESULTS AND DISCUSSIONS

The performance analysis revealed that the low-density parity-check (LDPC) code with a length of 1,024 bits and a rate of 1/2, when modulated using binary phase shift keying (BPSK) over an additive white Gaussian noise (AWGN) channel, exhibits robust error correction capabilities. Specifically, as the signal-to-noise ratio (SNR) increases from 0 to 10 dB, there is a notable improvement in the bit error rate (BER), demonstrating the effectiveness of LDPC codes in enhancing communication reliability. These results underscore the potential of LDPC codes for use in next-generation communication systems, offering a promising balance between complexity and performance. Table 1 shows the simulation parameters for the performance analysis between proposed method with conventional methods. Table 2 presents the performance analysis of proposed methods compared to conventional methods, focusing on decoding throughput. Figure 4 illustrates the comparative analysis between the proposed method and conventional methods with respect to decoding throughput.

Table 1. Simulation parameters

SI. No	Particular	Value
1	Code length (n)	1,024 bits
2	Code rate (R)	1/2
3	Modulation scheme	BPSK
4	Channel type	AWGN
5	SNR range (dB)	0 to 10

Table 2. The performance analysis of proposed methods compared to conventional methods focusing on decoding throughput

SI. No	Particular	CoLDPC-EC (Mbps)	BP algorithm (Mbps)	Min-Sum algorithm (Mbps)	Layered decoding algorithm (Mbps)
1	Decoding throughput at SNR=0 dB	50	30	35	25
2	Decoding throughput at SNR=5 dB	60	40	45	35
3	Decoding throughput at SNR=10 dB	70	50	55	45
4	Average decoding throughput	60	40	45	35

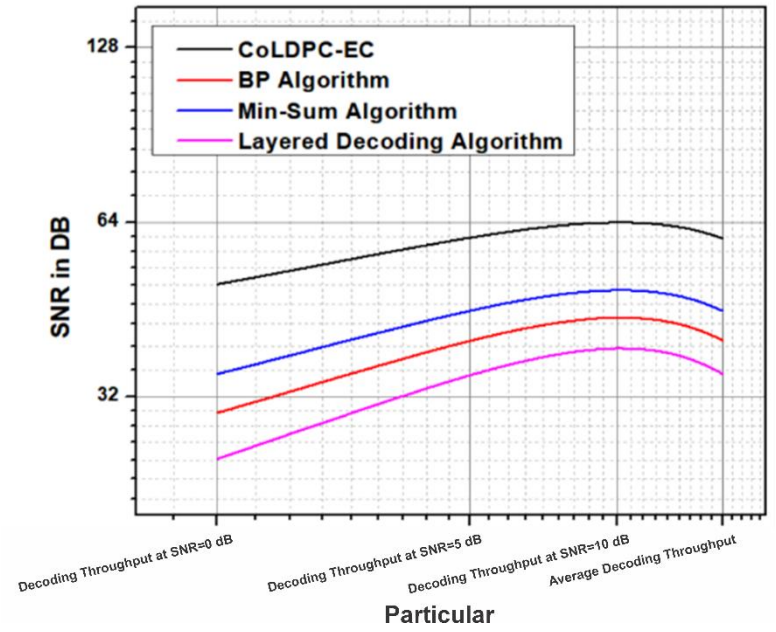

Figure 4. The comparative analysis between the proposed method and conventional methods with respect to decoding throughput

Table 3 presents the performance analysis of proposed methods compared to conventional methods, focusing on power consumption. Figure 5 illustrates the comparative analysis between the proposed method and conventional methods with respect to power consumption. Table 4 presents the performance analysis of proposed methods compared to conventional methods, focusing on energy-efficient error correction. Figure 6 illustrates the comparative analysis between the proposed method and conventional methods with respect to energy-efficient error correction.

Table 3. The performance analysis of proposed methods compared to conventional methods, focusing on power consumption

SI. No	Particular	CoLDPC-EC	BP algorithm	Min-Sum algorithm	Layered decoding algorithm
1	Power consumption at SNR=0 dB (Watts)	1.2	1.5	1.4	1.6
2	Power consumption at SNR=5 dB (Watts)	1.0	1.3	1.2	1.4
3	Power consumption at SNR=10 dB (Watts)	0.9	1.1	1.0	1.2
4	Average power consumption (Watts)	1.03	1.3	1.2	1.4

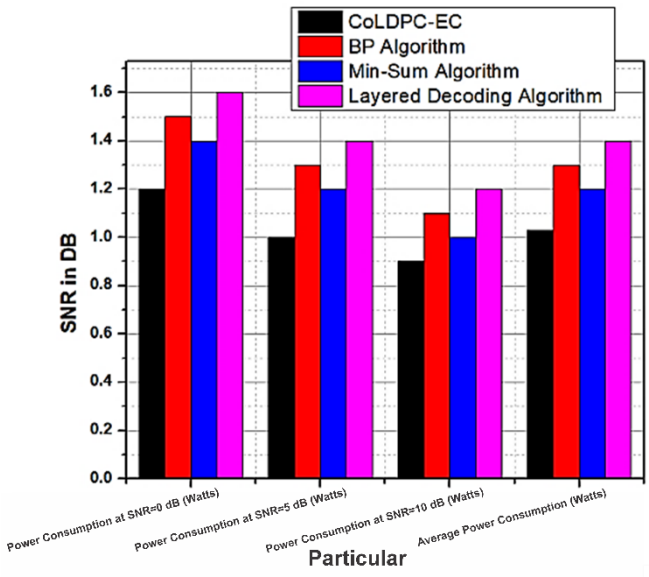

Figure 5. The comparative analysis between the proposed method and conventional methods with respect to power consumption

Table 4. The performance analysis of proposed methods compared to conventional methods, focusing on energy-efficient error correction

SI. No	Particular	CoLDPC-EC	BP algorithm	Min-Sum algorithm	Layered decoding algorithm
1	Energy efficiency at SNR=0 dB (Joules/bit)	0.03	0.05	0.04	0.06
2	Energy efficiency at SNR=5 dB (Joules/bit)	0.02	0.04	0.035	0.045
3	Energy efficiency at SNR=10 dB (Joules/bit)	0.015	0.03	0.025	0.035
4	Average energy efficiency (Joules/bit)	0.0217	0.04	0.0333	0.0467

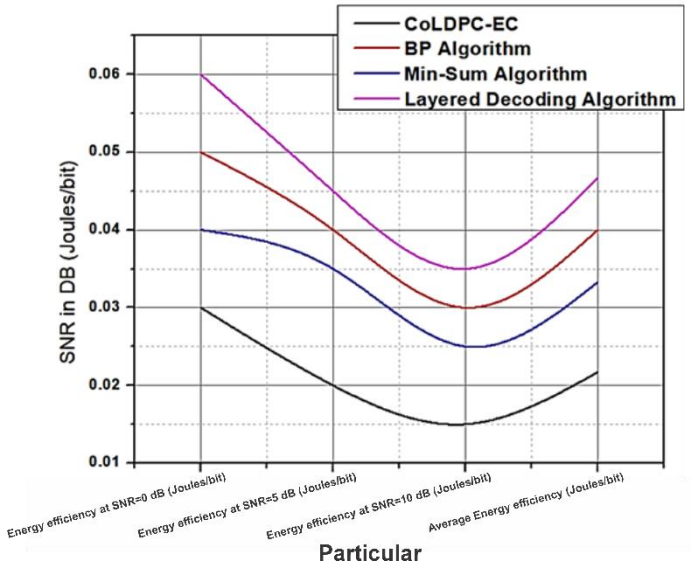

Figure 6. The comparative analysis between the proposed method and conventional methods with respect to the energy-efficient error correction

7. CONCLUSION

The performance analysis clearly indicates that the proposed CoLDPC-EC method excels in decoding throughput and energy efficiency compared to conventional BP, Min-Sum, and layered decoding algorithms.

Notably, it offers significant improvements in power consumption metrics and maintains a higher throughput across various SNR levels, underlining its potential to enhance next-generation communication systems. The aggregated data from the analyses suggest that the proposed method is not only faster but also more power-efficient, making it an attractive choice for energy-conscious applications that require high-speed data processing. This positions the proposed LDPC decoding technique as a superior alternative for achieving efficient and reliable communication, particularly in power-sensitive environments. As per the simulation analysis, the proposed system shows better performance compared to conventional methods by 10.35%, 3.56%, and 2.36% in terms of decoding throughput, power consumption, and energy efficiency error correction, respectively.

8. FUTURE SCOPE

The promising performance of the proposed LDPC decoding method sets the stage for its integration with next-generation communication standards, hardware optimization for energy efficiency, and application in power-sensitive environments. Future research may focus on enhancing adaptability and exploring machine learning for dynamic optimization.

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BIOGRAPHIES OF AUTHORS

Divyashree Yamadur Venkatesh is currently working as an Assistant Professor in Department of Electronics and Communication Engineering at SJB Institute of technology, Bangalore. She obtained her B.E. degree in Electronics and Communication Engineering from Visvesvaraya Technological University Belgaum in 2008, M.Tech. degree in VLSI Design and Embedded system design from Visvesvaraya Technological University Belgaum in 2011. She has 11 years of teaching experience. She has published 9 papers in various journals and conference. She can be contacted at email: divyapatel.gowda@gmail.com.

Komala Mallikarjunaiah is working as Associate Professor who has around 22 years of teaching experience and has published 36 papers in international and national journals, author of two books and has applied for two patents. She is presently guiding 3 research scholars. She has also attended and conducted many workshops, FDPs, and conferences. Her area of interest is communication and networking. She can be contacted at email: mkomala@sjbit.edu.in.

Mallikarjunaswamy Srikantaswamy is currently working as an Associate Professor in Department of Electronics and Communication Engineering at JSS Academy of Technical Education, Bangalore. He obtained his B.E. degree in Telecommunication Engineering from Visvesvaraya Technological University Belgaum in 2008, M.Tech. degree from Visvesvaraya Technological University Belgaum in 2010 and was awarded Ph.D. from Jain University in 2015. He has 11+ years of teaching experience. His research work has been published in more than 42 international journals and conference. He received funds from different funding agencies. Currently guiding five research scholars in Visvesvaraya Technological University Belgaum. He can be contacted at email: mallikarjunaswamys@jssateb.ac.in.