IAES International Journal of Artificial Intelligence (IJ-AI)
Vol. 14, No. 2, April 2025, pp. 1000~1021
ISSN: 2252-8938, DOI: 10.11591/ijai.v14.i2.pp1000-1021

Adaptive silicon synapse and CMOS neuron for neuromorphic VLSI computing

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Article Info

Article history:

Received Apr 14, 2024
Revised Nov 7, 2024
Accepted Nov 14, 2024

Keywords:

Adaptive silicon synapse
Neuromorphic computing
Spiking CMOS neuron
Spiking frequency modulation
Tuning synapse time-constant

ABSTRACT

The design of a fully integrated adaptive modified complementary metal-oxide-semiconductor (CMOS) synapse circuit is presented. By using multiple-gated transistor configuration in the modified CMOS synapse an additional branch provide control where the synaptic output current time-constant is tuned. The effect of changing the multiple-gated transistor bias voltage from 0.25 to 0.45 V tunes the spiking output current exponential time-constant range by 200 ms as shown in simulation results. Moreover, a fully-integrated adaptive quadratic integrate-and-fire (QIF) CMOS neuron circuit is presented as well. A differential pair with variable capacitor integrator and a tunable schmitt trigger threshold detector circuit are integrated in the CMOS neuron that can be tuned varying its spiking frequency. The proposed adaptive quadratic integrate-and-fire (AQIF) neuron has the ability to adjust the spiking frequency without changing the input current. The simulation results show the proposed CMOS neuron circuit spiking frequency can be tuned from 58.4 to 312.5 Hz and its spiking period from 17.1 to 3.2 ms with tuning the bias voltage of variable capacitor integrator. Having a peak voltage V_{peak}=0.95 V, a reset voltage V_{reset}=-0.75 V and a voltage threshold of 0.35 V with a membrane potential range of 1.5 V. The proposed CMOS neuron circuit is designed in 130 nm process with a supply voltage of 1.8 V and a total power dissipation of 1.8 mW.

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1. INTRODUCTION

In this paper, we present a fully integrated adaptive modified complementary metal-oxide-semiconductor (CMOS) synapse circuit is presented. By using multiple-gated transistor configuration in the modified CMOS synapse an additional branch provide control where the synaptic output current time-constant is tuned. The effect of changing the multiple-gated transistor bias voltage from 0.25 to 0.45 V increases the spiking output current exponentially by 0.5 mA and the decaying time-constant by 0.3 s as shown in simulation results. By tuning the decaying exponential time-constant with multiple-gated transistor configuration, the proposed modified CMOS synapse captures the dynamic nature of biological synapses. Merolla *et al.* [1] synapse design with feedback control achieved a tunable time-constant range is 100 ms. Hu *et al.* [2] design a memristor-based synapse with tunable time-constant range of 100 ms. Kwon *et al.* [3] synapse design with floating-gate has a 1 ms range of time-constant tuning. Tete *et al.* [4] synapse design

with varying capacitors achieved a tunable time-constant range of 10 us to 100 ms. Liu [5] design a memristor-based synapse with tunable time-constant range of 1 to 100 ms. Hong *et al.* [6] design a memristor-based synapse with tunable time-constant range of 100 us to 100 ms. Our proposed synapse design with multiple-gated transistor configuration achieved a tunable time-constant range of 200 ms compared to previously published work with limited tunable time-constant range to 100 ms. Moreover, a fully-integrated adaptive quadratic integrate-and-fire (AQIF) CMOS neuron circuit is presented as well. The proposed AQIF neuron has the ability to adjust the spiking frequency without changing the input current. The simulation results show the proposed CMOS neuron circuit spiking frequency can be tuned from 58.4 to 312.5 Hz and its spiking period from 17.1 to 3.2 ms with tuning the bias voltage of variable capacitor integrator. Having a peak voltage V_{peak}=0.95 V, a reset voltage V_{reset}=-0.75 V and a voltage threshold of 0.35 V with a membrane potential range of 1.5 V. The proposed AQIF neuron has the ability to adjust the spiking frequency without changing the input current. The proposed CMOS neuron number of transistors is 26 designed in 130 nm process with a supply voltage of 1.8 V and a total power dissipation of 1.8 mW. A spiking integrate-and-fire CMOS neuron is a type of artificial neuron that is designed to simulate the behavior of biological neurons using complementary CMOS technology [7].

The integrate-and-fire CMOS neuron circuits can be used in various applications such as neural network systems, neuromorphic computing [8]–[13] and brain-inspired computational systems [14]. A tunable spiking quadratic integrate-and-fire (QIF) neuron incorporates a quadratic function to model the non-linear behavior of biological neurons more accurately than integrate-and-fire CMOS neuron. Neuromorphic circuits, including QIF CMOS neurons, have gained significant interest in the field of artificial intelligence and neuroscience [15]–[18]. Due to their potential for high-speed, low-power, and parallel information processing, that makes them more efficient compared with Von Neumann bottleneck architecture [19]–[24]. The QIF CMOS neurons are typically implemented using CMOS technology. The QIF CMOS neuron can be used in various applications, including spiking neural networks (SNNs), neuromorphic computing and parallel computing architectures such as brain-machine interfaces [12], [25]–[28]. By accurately modeling the behavior of biological neurons, the spiking integrate-and-fire neuron can enable precise control of assistive technologies [3], [29]–[31]. Indiveri and Horiuchi [7] implemented an integrate-and-fire CMOS neuron using differential pair topology achieving low power consumption. They implemented his integrate-and-fire neuron in 800 nm CMOS process using 20 transistors. Srinivasan and Cowan [19] implemented his CMOS neuron using current-mode circuit topology with limited tunability capability. Qiao *et al.* [14] also designed his CMOS neuron using current-mode topology. Whereas Yu [29] implemented his neuron design using switch-capacitor circuit configuration. Wijekoon and Dudek [32] designed a QIF CMOS neuron in 350 nm process using 14 transistors. Sourikopoulos *et al.* [33] implemented an integrate-and-fire CMOS neuron in 65 nm process using 10 transistors. Whereas Schaik *et al.* [34] designed an Izhikevich CMOS neuron model in 90 nm process using 17 transistors. Indiveri and Liu [35] implemented his CMOS neuron using transconductance amplifier topology however it does not have circuit tunable capability. Moreover, Indiveri and Horiuchi [7] designed his integrate-and-fire neuron with membrane potential range of 1.5 V in 800 nm CMOS process however it does not have a tuning capability. Srinivasan and Cowan [19] designed his Izhikevich neuron with membrane potential range of 150 mV in 65 nm CMOS process with a frequency tuning range of 200 Hz. Ou and Ferreira [36] designed his Morris-Lecar neuron with membrane potential range of 200 mV in 180 nm CMOS process with a frequency tuning range of 290 Hz. Our proposed AQIF CMOS neuron has the ability to adjust the spiking frequency without changing the input current. The simulation results show that our proposed CMOS neuron spiking frequency can be tuned from 58.4 to 312.5 Hz and its spiking period from 17.1 to 3.2 ms with tuning the bias voltage of variable capacitor integrator. Having a peak voltage V_{peak}=0.95 V, a reset voltage V_{reset}=-0.75 V and a voltage threshold of 0.35 V with a membrane potential range of 1.5 V. The proposed AQIF neuron number of transistors is 26 designed in 130 nm CMOS process technology.

2. SPIKING NEURAL NETWORKS NEUROMORPHIC COMPUTATIONAL SYSTEM MODELING

SNN provides a promising solution for low-power hardware for neuromorphic computing. Using SNN circuit methods and doing parallel computations can reduce costs. SNN circuit functions with a pre-trained network's weights consume less power [7], [15], [37]–[41]. Biological neurons are in a network where a neuron receives input from another neuron. The inputs are received as a spike in the synapse. The in turn induce an output at the post synaptic. A SSN system consist of the following circuit building blocks as shown in Figure 1. The input receives the analog vector input signals [13], [38]. The weighted multiplication multiply the input vector elements by corresponding weights in an analog vector matrix multiplication (VMM). The analog VMM input is fed to a winner-take-all (WTA) circuit. The output from the WTA circuit is connected to a differential-pair integrator (DPI) synapse circuit [42], [43]. The DPI synapse circuit is then connected to an integrate-and-fire neuron. The output from the integrate-and-fire neuron is connected to the spike-timing

dependent plasticity (STDP) circuit as shown in Figure 1. The DPI synapse integrates the incoming signals [7], [37]–[39]. The WTA circuit selects the most active signal among neurons. The integrate-and-fire neuron integrates signals over time and generates output spikes. Then the STDP circuit adjusts synaptic weights based on the timing of spiking activity for learning and plasticity [13], [15], [40]–[44].

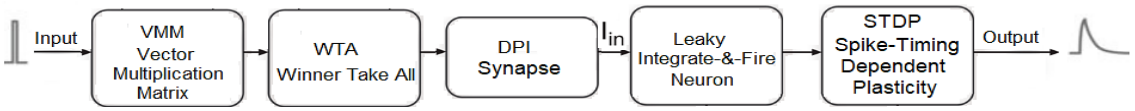

Figure 1. SSNs system

Analog very-large-scale integration (VLSI) is utilized to design SNNs circuits such as silicon synapse and CMOS neuron. Because transistors have properties similar to nerve membrane channels. When transistors are operated in weak inversion region, they leak a very small current. This transistor region of operation is also known as the subthreshold region. This way a large network of thousands of neurons will consume very low power. SNN do not fire continuously. SNN fires only when the post-synaptic potential reaches a certain threshold value. In the SNNs circuits the transistors are operating at the subthreshold level (weak inversion region). At this mode of operation, the current-voltage relationship is exponential and is best described by an exponential drain current equation plasticity [15], [40], [41]. Equations of subthreshold nfet transistor for a source follower circuit for SNN shown in Figure 2 can be described as (1) [4], [5], [38].

$$I = I_0 e^{\frac{\kappa V_g}{V_T}} \left(e^{-\frac{V_s}{V_T}} - e^{-\frac{V_d}{V_T}} \right) \quad (1)$$

Where I_0 is the current scale factor, V_T is the thermal voltage, V_g is the gate voltage, V_d is the drain voltage, and κ kappa is the capacitive divider and is given by (2) [4], [5], [38].

$$\kappa(\text{ kappa }) = \frac{\partial \psi_s}{\partial V_g} = \frac{C_{\text{ox}}}{C_{\text{ox}} + C_{\text{dep}}} \quad (2)$$

Equations of subthreshold pfet transistor for a source follower circuit for SNNs shown in Figure 2 can be described as (3) [4], [5], [38].

$$I = I_0 e^{-\frac{\kappa V_g}{V_T}} \left(e^{\frac{V_s}{V_T}} - e^{\frac{V_d}{V_T}} \right) \quad (3)$$

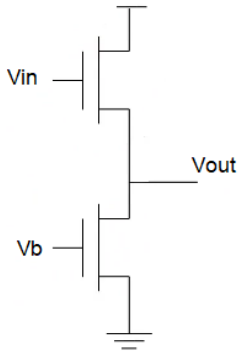

Figure 2. Source follower circuit for SNNs

Synapses are responsible for connecting neurons and communicating spike signals between them. A synapse receives spike voltages from the output of its pre-synaptic neuron. It produces a current based on a weight value [7], [37]–[40], [45]. Then it feeds this weighted current to its post-synaptic neuron [15], [41], [42], [44], [46], [47]. Exponentially decaying Log-domain Pulse Integrator circuit is shown in Figure 3. The linear integrator response is of a low-pass filter with a decaying exponential [7], [38], [48]–[50].

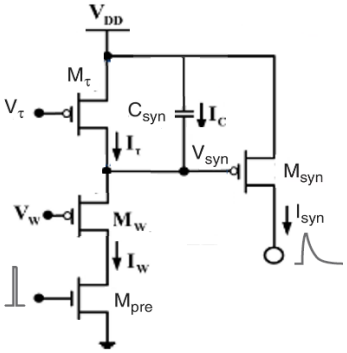

Figure 3. Log-domain pulse integrator circuit

By changing the bias voltage V_W shown in Figure 3 the synaptic weight can be varied. The current I_{syn} can be varied up and down exponentially with time as described in (4) [7], [38], [48]–[50].

$$I_{\text{syn}}(t) = \begin{cases} I_0 e^{+\frac{t}{\tau_c}} & \text{(charge phase for increasing current)} \\ I_0 e^{-\frac{t}{\tau_d}} & \text{(discharge phase for decreasing current)} \end{cases} \quad (4)$$

The I_0 is the initial current level, τ_c is the time-constant that determines how quickly the current rises, τ_d is the time-constant that determines how quickly the current falls and t is the time. In (5) and (6) describe the currents in sub-threshold mode of operation [5], [7], [13], [38], [42], [44], [51].

$$I_c = C\frac{d}{dt}(V_{dd} - V_{syn}) \quad (5)$$

$$I_{\text{syn}} = I_0 e^{\frac{\kappa(V_{dd}-V_{syn})}{V_T}} \quad (6)$$

Where I_c is the current through the capacitor and I_{syn} is the synapse output current in Figure 3. The derivative of the current through a capacitor can be determined in (7) where the larger the time-constant τ the larger the capacitor [5], [7], [13], [38], [42], [44], [51].

The solution for the first-order differential equation is given in (7). For a larger synapse weight we have to have a large I_W weight current [5], [7], [13], [38], [42], [44], [51].

$$I_w = I_0 e^{-\frac{\kappa(V_w - V_{\text{syn}})}{V_T}} \quad (7)$$

Where the I_0 is the initial current level, I_W is the weight current, V_W is the bias voltage, V_T is the thermal voltage, κ kappa is the capacitive divider and I_{syn} is the synapse output current. To get a larger synapse weight we can implement a DPI synapse circuit. The DPI synapse circuit is shown in Figure 4 [5], [7], [13], [38], [42], [44], [51].

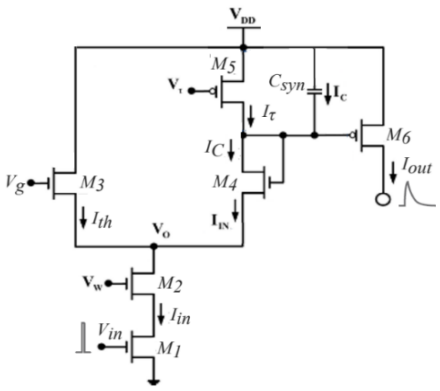

Figure 4. DPI synapse circuit

The DPI synapse integrates incoming signals as shown in the SNN system in Figure 1. It compares two input signals and generates an output based on their difference [5], [7], [13], [38], [42], [44], [51]. We can implement a DPI synapse by connecting the bulk of the pmos transistor to its source hence isolating its well. The capacitor C_{syn} voltage V_{syn} is shown in the circuit in Figure 4. The weighted contribution of a synapse can be implemented using a pmos transistor for excitator synapse and nmos for inhibitory synapse. In the DPI synapse, V_g controls the gain of the integration [5], [7], [13], [38], [42], [44], [51].

The current I_{in} is based on the assigned weight V_W. Then capacitor C_{syn} integrates current I_{in} and produce the gate voltage of transistor M6 shown in Figure 4. Voltage V_τ sets the time constant, and voltage V_g controls the gain of the integration as shown in Figure 4. The synapse output current I_{out} can be given by (8) [5], [7], [13], [38], [42], [44], [51].

$$I_{\text{out}} = I_0 e^{\frac{\kappa V_C}{V_T}} \tag{8}$$

Where the I_0 is the initial current level, V_c is the capacitor voltage, V_T is the thermal voltage, and κ kappa is the capacitive divider.

The DPI synapse circuit shown in Figure 4, to analyze the behavior of these synapses we can determine current equations in (9) and (10) [5], [7], [13], [38], [42], [44], [51].

$$I_{th} + I_C = I_{in} \tag{9}$$

$$I_C = I_{in} \times \frac{I_C}{I_{in}} = I_{in} \times \frac{I_C}{I_C + I_{th}} = \frac{I_{in}}{1+\frac{I_{th}}{I_C}} \tag{10}$$

Where I_{th} and I_{c} are sub-threshold currents controlled by the gate voltage of transistor M3 voltage V_g in Figure 4. The sub-threshold currents can be described in (11)-(13) [5], [7], [13], [38], [42], [44], [51].

$$I_C = I_0 e^{\frac{\kappa V_C}{V_T}} \tag{11}$$

$$I_{th} = I_0 e^{\frac{\kappa V_g}{V_T}} \tag{12}$$

$$I_C = \frac{I_{in}}{1+e^{\frac{\kappa(V_g - V_C)}{V_T}}} \tag{13}$$

Where I_{c} sub-threshold current of capacitor C_{syn}. The output current I_{out} and I_{c} sub-threshold current of capacitor C_{syn} can be defined as a function of output current I_{out} and I_g as (14)-(16) [5], [7], [13], [38], [42], [44], [51].

$$I_{\text{out}} = I_0 e^{-\frac{\kappa(V_C - V_{DD})}{V_T}} \tag{14}$$

$$I_g = I_0 e^{-\frac{\kappa(V_g - V_{DD})}{V_T}} \tag{15}$$

$$I_C = \frac{I_{\text{in}}}{1+\frac{I_{\text{out}}}{I_g}} \tag{16}$$

Where I_g is the sub-threshold current of a pmos transistor M3 with the gate voltage V_g and current I_{out} of transistor M6 is shown in Figure 4.

The derivative of the output current I_{out} can be defined as (17)-(19) [5], [7], [13], [38], [42], [44], [51].

$$I_{\text{out}} = I_0 e^{-\frac{\kappa(V_C - V_{DD})}{V_T}} \tag{17}$$

$$\frac{d}{dt} I_{out} = I_0 e^{-\frac{\kappa(V_C - V_{DD})}{V_T}} \times \frac{d}{dt}\left(-\frac{\kappa(V_C - V_{DD})}{V_T}\right) \tag{18}$$

$$\frac{d}{dt} I_{\text{out}} = I_{\text{out}} \times \left(-\frac{\kappa}{V_T}\right) \frac{d}{dt} V_C \tag{19}$$

Where derivative of the capacitor voltage $\frac{d}{dt} V_C$ can be determined from capacitor C_{syn} current in Figure 4 [5], [7], [13], [38], [42], [44], [51].

$$C_{\text{syn}} \frac{d}{dt} V_C = I_\tau - I_C \Rightarrow \frac{d}{dt} V_C = \frac{I_C - I_\tau}{C_{\text{syn}}} \quad (20)$$

The resulting differential equation is as (21).

$$\frac{d}{dt} I_{\text{out}} = \left(\frac{\kappa I_\tau}{U_T C_{\text{syn}}}\right)\left(\frac{\frac{I_{\text{in}}}{I_\tau}}{1+\frac{I_{\text{out}}}{I_g}} - 1\right) \times I_{\text{out}} \quad (21)$$

Where τ is the time-constant and if gate voltage V_g is greater than the capacitor voltage V_C, the differential equation of the filter can be described as a first-order low-pass filter differential equation as (22). The DPI synapse with current source circuit as shown in Figure 5.

$$\tau \frac{d}{dt} I_{out} + I_{out} = \frac{I_{in} I_g}{I_\tau} \quad (22)$$

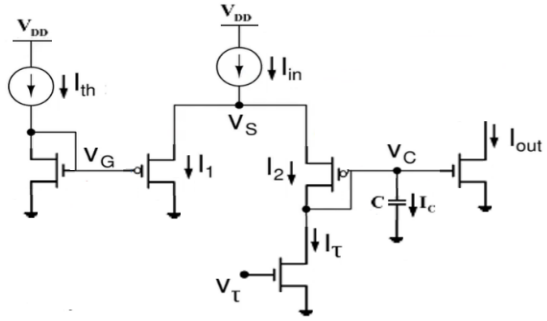

Figure 5. DPI synapse with current source circuit

The output current I_{out} can be determined as (23) and (24).

$$\text{rise } \Rightarrow I_{\text{out}}(t) = \frac{I_{\text{in}} I_g}{I_\tau}\left(1 - e^{-\frac{t-t^+}{\tau}}\right) + I_{\text{out}}(t^+) e^{-\frac{t-t^+}{\tau}} \quad (23)$$

$$\text{decay } \Rightarrow I_{\text{out}}(t) = I_{\text{out}}(t^+) e^{-\frac{t-t^+}{\tau}} \quad (24)$$

Where $I_{\text{out}}(t^+)$ is the output current value in spike arrival time. The time-constant τ is of this filter depends on the value of the capacitor and voltage V_τ. In the filter circuit the values of voltage V_g and voltage V_W control the filter gain [5], [7], [13], [38], [42], [44], [51].

Combining a WTA circuit with a DPI synapse and a leaky integrate-and-fire (LIF) neuron can create a sophisticated neural networks architecture as shown in the SSNs in Figure 1. WTA circuit can be implemented with connecting to or more current conveyers as shown in Figure 6. The WTA circuit select the synapse with the highest input signal strength wins and suppresses the activity of the other synapse [5], [7], [13], [38], [42], [44], [51].

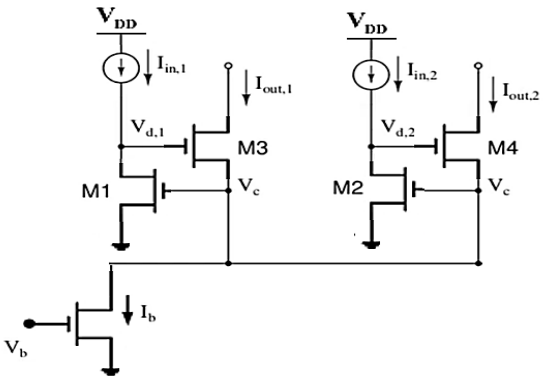

Figure 6. WTA circuit

The input receives the analog vector input signals. The weighted multiplication multiply the input vector elements by corresponding weights in the analog VMM. The summation sum up the weighted products to get the final output [6], [52], [53]. The analog VMM input is fed to and is connected to the WTA circuit. The output provides the result of the VMM for further processing in the neural networks. The analog VMM circuits shown in Figure 7 can process multiple elements of the input vector simultaneously enabling parallel computation [6], [52], [53].

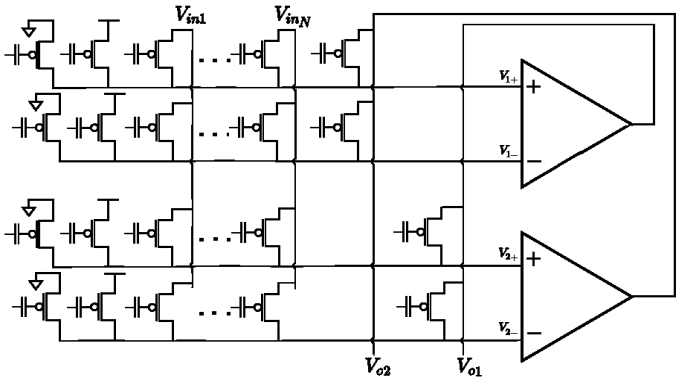

Figure 7. Analog VMM circuit

The STDP circuit is located in the learning plasticity module of the neural networks system as shown in Figure 1 [6], [7], [37], [38], [50]–[53]. The STDP circuit adjust the synaptic weights based on spike timing. The capacitor is used for comparing spike timings. The STDP circuit is typically located after the DPI synapse, WTA circuit, and LIF neuron in the block diagram as shown in Figure 8.

The STDP circuit shown in Figure 8 detects spikes from the pre-synaptic neuron. It triggers when the pre-synaptic voltage crosses a threshold. The STDP circuit measures the timing difference between the pre-synaptic and post-synaptic spikes. Then integrates the synapse current and adjusts the synaptic weight based on the timing information [5]–[7], [13], [37], [38], [42], [44], [50]–[53].

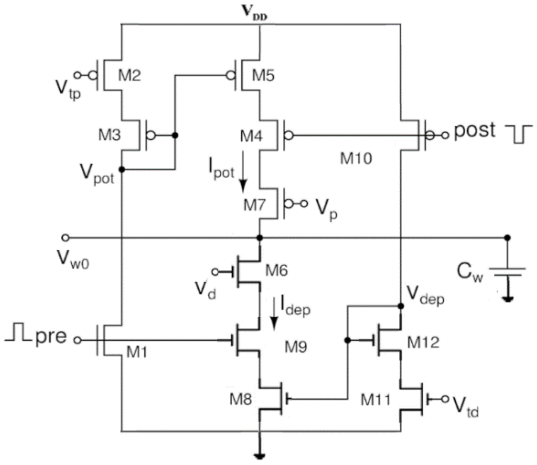

Figure 8. STDP circuit

3. A CMOS SYNAPSE CIRCUIT MODEL FOR SSN

Synapses are responsible for connecting neurons and communicating spike signals between them. A synapse receives spike voltages from the output of its pre-synaptic neuron. It produces a current based on a weight value. Then it feeds this weighted current to its post-synaptic [5]–[7], [13], [37], [38], [42], [44], [50]–[53]. A CMOS synapse circuit model for SSNs is shown in Figure 9. The CMOS synapse circuit design ensure that all transistors are working at the subthreshold level [4], [5], [50].

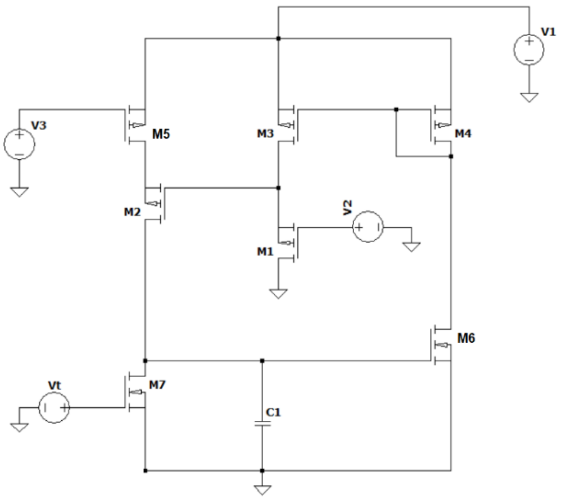

Figure 9. A CMOS synapse circuit model for SNN

A CMOS synapse circuit model for SNN time-constant τ_d can be described in (25) [4], [5], [50].

$$\tau_d = \frac{CV_T}{k_n I_\tau} \tag{25}$$

Where τ_d is the synapse time-constant and V_T is the thermal voltage, C is the capacitor C1 in synapse circuit shown in Figure 9, $k_n = \mathrm{Wn/Ln}$ is the transistor width to length ratio parameter, and I_τ the sub-threshold drains current of transistor M7 in Figure 10.

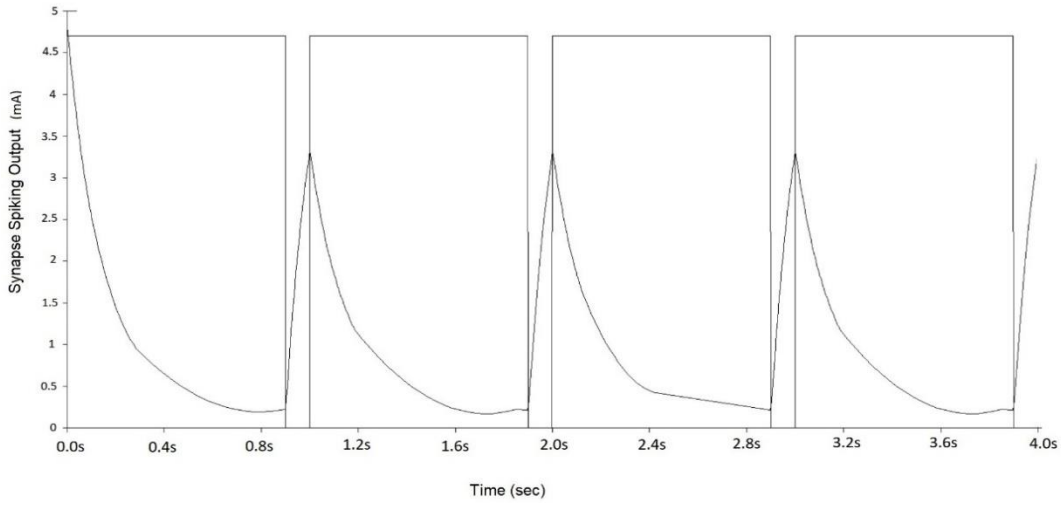

Figure 10. The CMOS synapse circuit model for SNNs simulation results

Figure 9 shows the CMOS synapse circuit model for SSNs. The design ensure that all transistors are working at the subthreshold level similar to the model provided by studies [7], [35], [38]. In the circuit shown in Figure 9, the current through transistor M7 shown in Figure 9 was the determinant factor to control the time-constant parameter. The CMOS synapse circuit model for Spiking simulation results is shown in Figure 10. Using multiple-gated transistors configuration M8 and M9 transistors, an additional branch parallel to transistor M7 provided additional control where the synaptic output time-constant can be tuned. Figure 11 shows the proposed modified adaptive CMOS synapse circuit SNN model with time-constant parameter tuning.

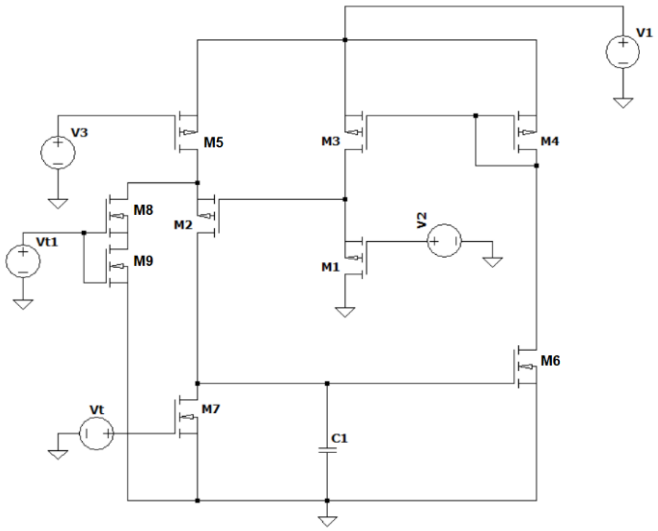

Figure 11. The proposed modified adaptive CMOS synapse circuit SNN model with time-constant tuning

The transistors are operating at the subthreshold level weak inversion region. At this mode of operation, the current-voltage relationship is exponential where V_T is the thermal voltage, $k_n = \mathrm{Wn/Ln}$ is the transistor width to length ratio parameter and C1 is the capacitor in synapse circuit shown in Figure 11.

Using Kirchoff's current law we get (26) and (27) [4], [5], [50].

$$i_c = i_2 - i_\tau \tag{26}$$

knowing that [4], [5], [50].

$$i_c = C\frac{dV_c(t)}{dt} \tag{27}$$

Substituting (26) in (27) we get (28) [4], [5], [50].

$$C\frac{dV_c(t)}{dt} = SI_o e^{\frac{k_p}{V_T}(V_{dd}-V_w)} - I_\tau \tag{28}$$

I_τ the sub-threshold drain current of transistor M7 in Figure 11 can be determined by substituting (27) in (28) we get (29) and (30) [4], [5], [50].

$$I_\tau = S_7 I_o e^{\frac{V_\tau}{V_T}k_n} \tag{29}$$

$$i_{synapse}(t) = S_8 I_o e^{\frac{k_n}{V_t}v_c(t)} \tag{30}$$

Taking the derivative of $i_{synapse}$ synapse current we get (31) [4], [5], [50].

$$\frac{d_{i_{synapse}}(t)}{dt} + \frac{k_n I_\tau}{CV_T} i_{synapse(t)} = \frac{S_8 k_n I_o}{CV_T} e^{\frac{k_p}{V_T}(V_{dd}-V_w)} \tag{31}$$

The synapse time constant τ can be determined by (32) [4], [5], [50].

$$\tau = \frac{CV_T}{K_n I_\tau} \tag{32}$$

Where τ is the synapse time-constant and V_T is the thermal voltage, C is the capacitor C1 in synapse circuit shown in Figure 9, $k_n = \mathrm{Wn/Ln}$ is the transistor width to length ratio parameter and I_τ the sub-threshold drains current of transistor M7 in Figure 11.

The modified CMOS synapse circuit shown in Figure 11 time-constant τ_r is given by (33) [4], [5], [50].

$$\tau_r = \frac{CV_T}{k_n(I_{\tau r}+I_\tau)} \quad (33)$$

Where τ_r is the modified synapse circuit time-constant and V_T is the thermal voltage, C1 is the capacitor in synapse circuit shown in Figure 11, $k_n = \mathrm{Wn/Ln}$ is the transistor width to length ratio parameter, I_τ the sub-threshold drains current of transistor M7 and $(I_{\tau r} + I_\tau)$ is the total sub-threshold drain current of the multiple-gated transistor M8, M9, and M7 shown in Figure 11. By using multiple-gated transistors configuration M8 and M9 transistors, an additional branch parallel to transistor M7 provide additional control where the synaptic output time-constant is tuned.

The simulation results shown in Figure 12 illustrate the tuning of the modified CMOS synapse circuit time-constant parameter. By using multiple-gated transistors configuration M8 and M9 transistors, an additional branch parallel to transistor M7 shown in Figure 11 provide additional control where the synaptic output time-constant is tuned. The effect of changing multiple-gated transistors bias voltage on the decaying time-constant from V_{t1}=0.25 V bias voltage to V_{t1}=0.3 V and to V_{t1}=0.45 V is shown in Figure 12. By using multiple-gated transistor configuration in the modified CMOS synapse the synaptic output current time-constant is tuned. The effect of changing the multiple-gated transistor bias voltage from 0.25 to 0.45 V tunes the spiking output current exponential time-constant range by 200 ms as shown in simulation results in Figure 12. By tuning the decaying exponential time-constant with multiple-gated transistor configuration, the proposed modified CMOS synapse captures the dynamic nature of biological synapses. Table 1 shows the adaptive modified CMOS synapse circuit transistor dimensions width and length. Table 2 shows the tunable of time-constant range of previously published synapse designs in comparison to the proposed synapse design. Our proposed synapse design with multiple-gated transistor configuration achieved a tunable time-constant range of 200 ms compared to previously published work with limited tunable time-constant range to 100 ms.

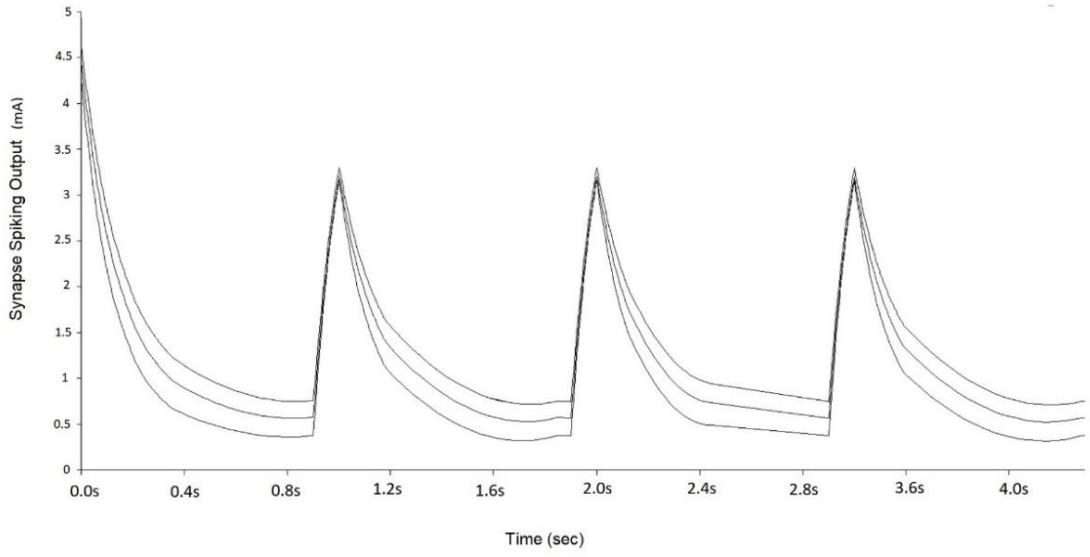

Figure 12. The modified adaptive CMOS synapse circuit SNN model with time-constant tuning

Table 1. Adaptive modified CMOS synapse transistor dimensions

Transistor dimensions	Length	Width
M1	2	4
M2	5	10
M3	5	15
M4	5	10
M5	5	10
M6	5	10
M7	5	10
M8	5	15
M9	5	15

Table 2. Synapse design tunable time-constant range comparison

Synapse design	Circuit configuration	Time-constant tuning range
Merolla *et al.* [1]	Feedback control	100 ms
Hu *et al.* [2]	Memristor-based	100 ms
Kwon *et al.* [3]	Floating-gate	1 ms
Tete *et al.* [4]	Varying capacitors	10 us to 100 ms
Liu [5]	Memristor-based	1 ms to 100 ms
Hong *et al.* [6]	Memristor-based	100 us to 100 ms
This Work	Multiple-gated	200 ms

4. SPIKING INTEGRATE-AND-FIRE CMOS NEURON

A spiking integrate-and-fire CMOS neuron is a type of artificial neuron that is designed to simulate the behavior of biological neurons using CMOS technology [7], [38]. The integrate-and-fire CMOS neuron circuits can be used in various applications such as neural network systems, neuromorphic computing [8], [10]–[12], [34], [44], [54], [55] and brain-inspired computational systems [14]–[16]. A tunable spiking QIF neuron incorporates a quadratic function to model the non-linear behavior of biological neurons more accurately than integrate-and-fire CMOS neuron. Neuromorphic circuits, including QIF CMOS neurons, have gained significant interest in the field of artificial intelligence and neuroscience [17], [56]. Due to their potential for high-speed, low-power, and parallel information processing, that makes them more efficient compared with Von Neumann bottleneck architecture [20]–[24], [34], [37], [48]–[50].

The QIF CMOS neurons are typically implemented using CMOS technology. QIF CMOS neuron can be used in various applications, including SNNs, neuromorphic computing and parallel computing architectures such as brain-machine interfaces [12], [25]–[28]. By accurately modeling the behavior of biological neurons, the spiking integrate-and-fire neuron can enable precise control of assistive technologies [3], [29]–[31], [33], [40], [43]. In studies [7], [38] implemented an integrate-and-fire CMOS neuron using differential pair topology achieving low power consumption. In studies [7], [38] implemented his integrate-and-fire neuron in 800 nm CMOS process using 20 transistors. Schaik *et al.* [34] implemented his CMOS neuron using current-mode circuit topology with limited tunability capability. Qiao *et al.* [14] also designed his CMOS neuron using current-mode topology. Whereas in studies [29], [43] implemented his neuron design using switch-capacitor circuit configuration. Indiveri *et al.* [45] designed a QIF CMOS neuron in 350 nm process using 14 transistors. In studies [31], [33] implemented an integrate-and-fire CMOS neuron in 65 nm process using 10 transistors. Whereas Schaik *et al.* [34] designed an Izhikevich CMOS neuron model in 90 nm process using 17 transistors. Indiveri and Liu [35] implemented his CMOS neuron using transconductance amplifier topology however it does not have circuit tunable capability. Moreover, Indiveri *et al.* [38] designed his integrate-and-fire neuron with membrane potential range of 1.5 V in 800 nm CMOS process however it does not have a tuning capability. Van Schaik *et al.* [34] designed his Izhikevich neuron with membrane potential range of 150 mV in 65 nm CMOS process with a frequency tuning range of 200 Hz. Ou and Ferreira [36] designed his Morris-Lecar neuron with membrane potential range of 200 mV in 180 nm CMOS process with a frequency tuning range of 290 Hz.

5. LEAKY INTEGRATE-AND-FIRE CMOS NEURON MODEL

A LIF neuron model includes a leak term to the membrane potential that reflects the diffusion of ions that occurs through the membrane when some equilibrium is not reached in the cell [57], [58]. The LIF neuron model consist of a capacitor C in parallel with a resistor R driven by a current I(t). The driving current is split into two components and is described in (34) [54], [57]–[60].

$$I(t) = I_R - I_C \tag{34}$$

Where I(t) is the input current injected to the neuron and I_R is the current that flows through its membrane resistor and I_C is the current that flows through its circuit capacitor representing the neuron membrane capacitor.

Rearranging (1) with Ohms law and the capacitor current, we get (35).

$$I(t) = \frac{V_{mem}}{R} + C.\frac{dV_{mem}}{dt} \tag{35}$$

Multiplying (2) with R and introducing τ neuron membrane time constant, the (35) becomes (36) [57], [58].

$$\tau.\frac{dV_{mem}}{dt} = -V_{mem} + R.I(t) \tag{36}$$

Where V_{mem} is the neuron membrane potential.

Figure 13 shows a LIF CMOS neuron model including its circuit capacitor representing the neuron membrane capacitor. The input current I_{in} injected to the neuron flowing through transistor M1 in Figure 13 can be described as (37) [54], [57]–[60].

$$I_{in} = I_{th} e^{\frac{K(V_{dd}-V_{in}-V_{T0}))}{V_T}} \left(1 - e^{\frac{-(V_{dd}-V_{mem})}{V_T}}\right) \quad (37)$$

The leak current I_{leak} injected to the neuron flowing through transistor M2 in Figure 13 can be described as (38) [57]–[59].

$$I_{leak} = I_{th} e^{K(V_t-V_1-V_{T0})} \left(1 - e^{\frac{-(V_{mem}-V_1)}{V_T}}\right) \quad (38)$$

Adding both currents by taking the current node equation between M1 and M2, the current flowing through the membrane capacitance can be described as (39).

$$\left(\frac{dV}{dt} V_{mem}\right)\left(C_{mem} + C_f\right) = I_{in} - I_{leak} \quad (39)$$

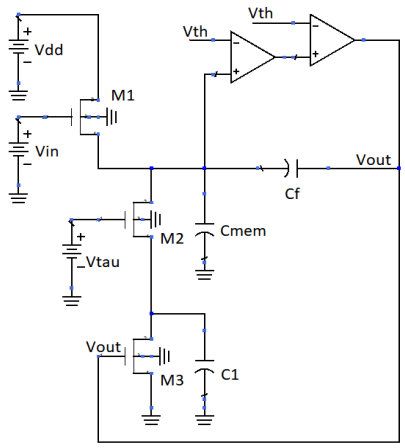

Figure 13. Modeling a LIF CMOS neuron

In a LIF CMOS neuron model, the neuron will fire when the input current I exceeds the threshold current, otherwise it will leak out any potential change. It exhibits periodic spiking T [57]–[59].

$$T = \tau \, ln\left(\frac{RI_o}{RI_o - V_{th}}\right) \quad (40)$$

Where τ is the time constant of the circuit and V_{th} is the threshold voltage. Since there is a spike every time the capacitance discharges, the spike firing frequency f is the reciprocal of time T and the spike firing frequency f can be described as (41).

$$f = \frac{1}{\tau \, ln\left(\frac{RI_o}{RI_o - V_{th}}\right)} \quad (41)$$

Figure 14 shows a MATLAB simulation of a LIF membrane potential with constant input current. Figure 15 shows a Tensorflow python simulation of a LIF membrane potential with constant input current. Figure 16 shows another implementation of a LIF subthreshold CMOS neuron circuit [61].

In Figure 16, the current flowing through membrane capacitance Cv can be described as (42).

$$\left(Cv \frac{dV}{dt}\right) = I_{M3} - I_{M5} + I_{syn} \quad (42)$$

Whereas the current flowing the circuit capacitance C_U can be described as (43).

$$\left(C_U \frac{dV}{dt}\right) = I_{M4} - I_{M6} \quad (43)$$

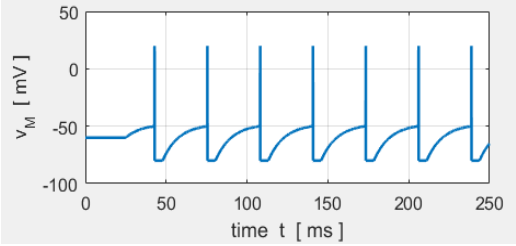

Figure 14. MATLAB simulation of a LIF membrane potential with constant input current

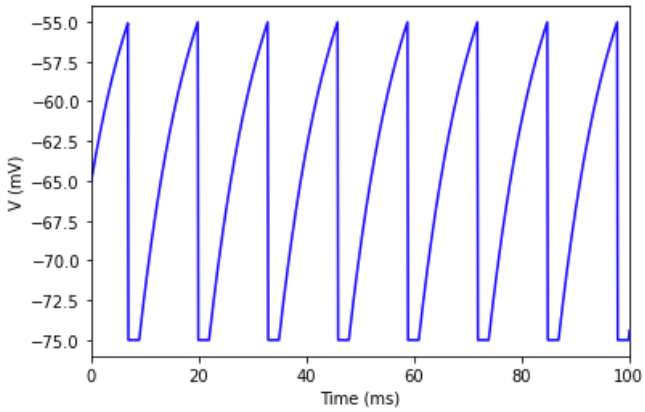

Figure 15. Tensorflow python simulation of a LIF membrane potential with constant input current

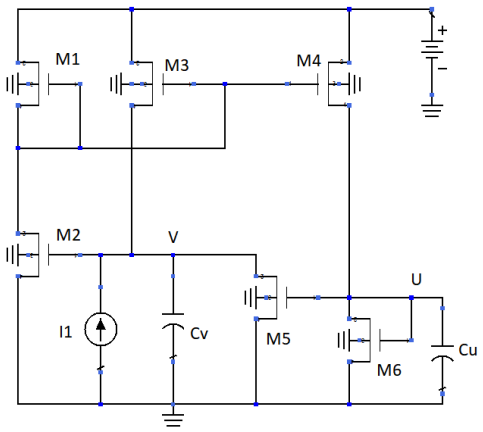

Figure 16. A LIF subthreshold CMOS neuron implementation [61]

6. QIF CMOS NEURON MODEL

The QIF neuron model is described by the following differential equation in (44) [10], [16], [54], [59], [60], [62].

$$\frac{dV}{dt} = (V - V_{reset})(V - V_{th}) + I \tag{44}$$

Where dV/dt is the rate of change of the membrane potential and V is the membrane potential. V_{reset} is the reset potential. V_{th} is the threshold potential, and I is the input current [10], [16], [54], [59], [60], [62].

The QIF neuron model can be rearranged into (45). R and C being the resistance and capacitance respectively of the QIF neuron circuit integrator [54], [59], [60], [62].

$$RC\frac{d}{dt}V = V^2 + I \tag{45}$$

The quadratic term captures the neuron firing rate nonlinear quadratic behavior. The QIF neuron model can be implemented as an analog circuit implementation where V is the voltage across the cell membrane and I is the input current with a given reset condition described as (46) [15], [58], [60], [62], [63].

$$V = \frac{1}{RC}\int V^2 + I \text{ When } V>V_{peak} \text{ then } V=V_{reset} \tag{46}$$

The QIF neuron model exhibits a periodic spiking T that can be described as (47) [54], [59], [60], [62], [64].

$$T = \frac{1}{2\sqrt{I}}\ln\left(\frac{(V_{peak}-\sqrt{I})(V_{reset}+\sqrt{I})}{(V_{peak}+\sqrt{I})(V_{reset}-\sqrt{I})}\right) \tag{47}$$

Where the V_{peak} is the peak membrane potential and V_{reset} is the reset potential, and I is the input current.

$$\log(\lambda) = \frac{2ra}{\sigma_n^2} \tag{48}$$

7. PROPOSED ADAPTIVE QUADRATIC INTEGRATE-AND-FIRE CMOS NEURON

The proposed AQIF CMOS neuron is shown in Figure 17. A differential pair with variable capacitor integrator (Figure 17(a)), voltage amplifier (Figure 17(b)), variable diode capacitor (Figure 17(c)), a tunable schmitt trigger threshold detector circuit (Figure 17(d)) and a switch metal oxide semiconductor field effect transistor (MOSFET) transistor are integrated in the AQIF CMOS neuron which models the quadratic neuron behavior. The proposed AQIF CMOS neuron has the ability to adjust the spiking frequency without changing the input current.

The QIF CMOS neuron dynamics is represented in the form of a differential equation describing the action potential of the neuron as (49) [39], [40], [51], [60], [62], [64], [65].

$$C_m\frac{dV}{dt} = g_L\frac{(V-V_{th})(V-V_{reset})}{(V_{th}-V_{reset})} + I \tag{49}$$

Where C_m is the membrane capacitance, V_{th} is the threshold potential, V_{reset} is the reset potential, I is the input current, and g_L is the leak conductance. The rate of change of the membrane potential $\frac{dV}{dt}$ is determined by the input current I, leak conductance g_L, and the equation quadratic term $\frac{(V-V_{th})(V-V_{reset})}{(V_{th}-V_{reset})}$. This quadratic term introduces nonlinearity into the neuron's dynamics resulting in its spiking behavior.

The AQIF CMOS neuron membrane time constant τ, near threshold voltage, can be described as (50) [39], [40], [45], [62], [65]–[67].

$$\tau = \frac{C(V_{th}-V_{reset})}{g_L(V_{th}+V_{reset})} \tag{50}$$

The AQIF CMOS neuron exhibits firing rate f as a function of input current I to the neuron [9], [41], [55], [57], [60], [68]–[71].

$$f = \frac{2\sqrt{I}}{\tau.(V_{th}-V_{reset}).\ln\left(\frac{(V_{th}-V_{mem})+\sqrt{I})}{(V_{reset}-V_{mem})+\sqrt{I}))}\right)} \tag{51}$$

Where τ is the neuron membrane time constant and R is the membrane resistance and C is the neuron membrane capacitance. V_{mem} represents the membrane potential of the AQIF CMOS neuron, V_{th} is the threshold potential at which the neuron fires an action potential, V_{reset} is the reset potential after a spike occurs, I is the input current to the neuron, and τ is the time constant associated with the neuron membrane potential [37], [38], [72]–[75].

The proposed AQIF CMOS neuron shares the ability to adjust its parameters to control its behavior and response characteristics. The differential amplifier integrator (M4-M8) circuit is coupled with a variable diode capacitor (M13-M18) circuit as shown in Figure 17. The variable diode capacitor is placed between the integration stage and the tunable Schmitt trigger (M19-M26) circuit. The positive feedback occurs through

the quadratic nonlinearity introduced by the nonlinear element switch MOSFET M2 operating in the saturation region to implement the quadratic dynamics of the CMOS neuron.

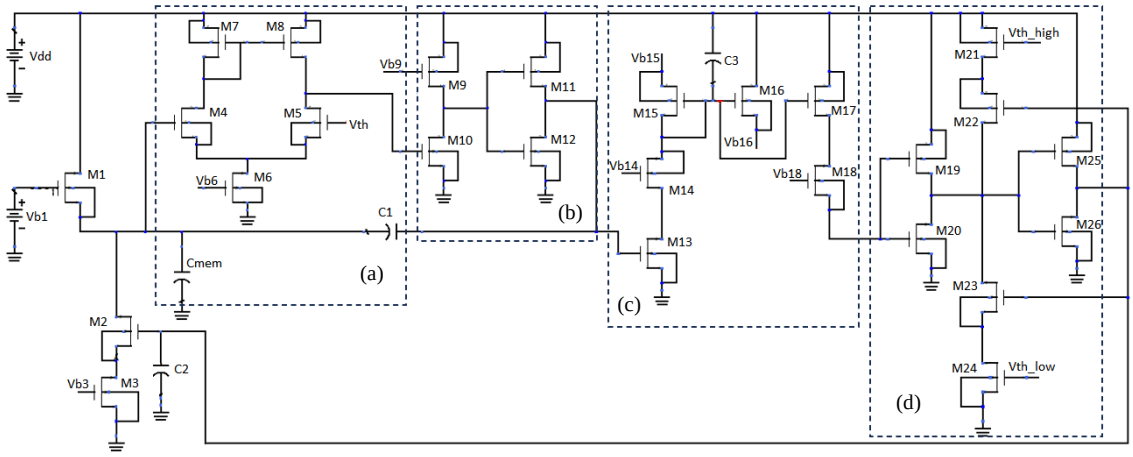

Figure 17. Proposed AQIF CMOS neuron of (a) differential pair integrator, (b) voltage amplifier, (c) variable diode capacitor, and (d) tunable schmitt trigger

The integrated output voltage, which represents the membrane potential, is fed into the variable diode capacitor. The variable diode capacitor is a circuit that uses a diode transistor M15 and a capacitor C3 of 1nF in conjunction. The diode transistor M15 acts as a variable resistor, allowing the time constant to be changed by varying the diode transistor bias voltage.

The membrane time constant $\tau = \frac{C(V_{th}-V_{reset})}{g_L(V_{th}+V_{reset})}$ in (14) the parameter that can be varied by the variable diode capacitor is the leak conductance g_L. The variable diode capacitor circuit allows for the adjustment of the time constant τ by changing the bias voltage of the diode transistor M15. In the (14), the membrane time constant τ is inversely proportional to the leak conductance g_L.

By adjusting the bias voltage of the diode in the variable diode capacitor integrator circuit, the effective leak conductance can be adjusted, resulting in a corresponding change in the time constant of the circuit. Therefore, by varying the diode bias voltage V_{bias} in the variable diode capacitor integrator, the time constant τ can be tuned to achieve the desired spike frequency behavior of the circuit as shown in (52).

$$V_{bias} = \frac{\tau g_L(V_{th}+V_{reset})}{C+V_{th}-V_{reset}} \quad (52)$$

Therefore, to achieve a time constant of 3.2 ms corresponding to spike frequency 312.5 Hz, the variable diode capacitor bias voltage in the circuit is adjusted to 1.1 V as shown in Table 3. To achieve a time constant of 17.1 ms corresponding to spike frequency 58.4, the variable diode capacitor bias voltage in the circuit is adjusted to 0.9 V as shown in Table 4.

Table 3. Variable capacitor integrator bias voltage tuning for spike frequency 312.5 Hz

Parameter	Value
Membrane time constant τ	3.2 ms
Leak conductance g_L	100 µS
Threshold potential V_{th}	0.35 V
Reset potential V_{reset}	-0.75 V
Bias Voltage V_{bias}	1.1 V

Table 4. Variable capacitor integrator bias voltage tuning for spike frequency 58.4 Hz

Parameter	Value
Membrane time constant τ	17.1 ms
Leak conductance g_L	100 µS
Threshold potential V_{th}	0.35 V
Reset potential V_{reset}	-0.75 V
Bias Voltage V_{bias}	0.9 V

The output of the variable diode capacitor is passed to the tunable Schmitt trigger (M19-M26) circuit, which compares the voltage with adjustable threshold levels to generate the output spike when the upper threshold is reached. The tunable Schmitt trigger circuit is set with the upper threshold $V_{th_{high}}$ to

0.35 V and the lower threshold $V_{th_{low}}$ is set to -0.2 V as shown in Table 5. The membrane potential gradually increases due to the injected current. It continues to rise until it reaches the upper threshold $V_{th_{high}}$. When the membrane potential V exceeds the upper threshold $V_{th_{high}}$ of 0.35 V, the Schmitt trigger CMOS circuit detects this and generates a positive spike or action potential. After generating the spike, the membrane potential is reset to the reset potential V_{reset} of -0.75 V to simulate the refractory period of the neuron.

The membrane potential starts to integrate incoming currents again until it reaches the lower threshold $V_{th_{low}}$ of -0.2 V. As the membrane potential gradually increases, the Schmitt trigger circuit detects the crossing of $V_{th_{low}}$ of -0.2 V and generates another positive spike indicating another action potential. As the membrane potential crosses, the upper threshold, this process repeats generating action potentials at regular intervals as shown in Figures 18 and 19.

Table 5. Tunable CMOS Schmitt trigger parameters

Parameter	Value
Upper threshold potential $V_{th_{high}}$	0.35 V
Lower threshold potential $V_{th_{low}}$	-0.2 V
Reset potential V_{reset}	-0.75 V

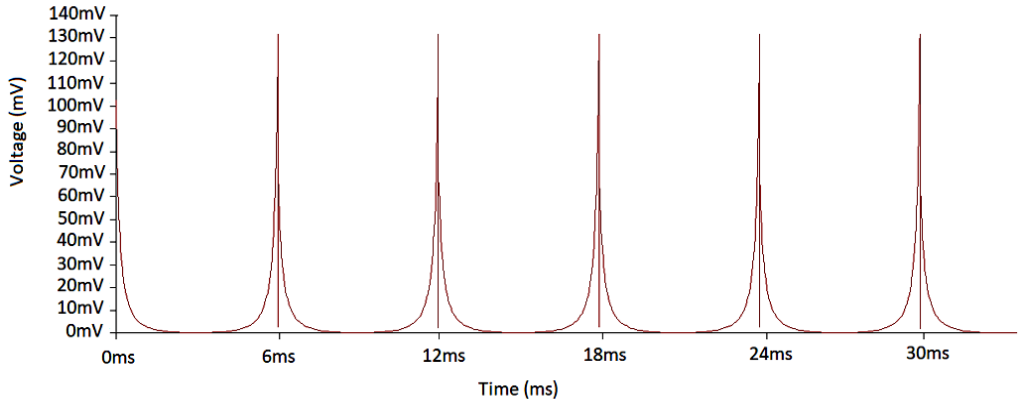

Figure 18. Simulation results for the AQIF CMOS neuron circuit quadratic voltage behavior

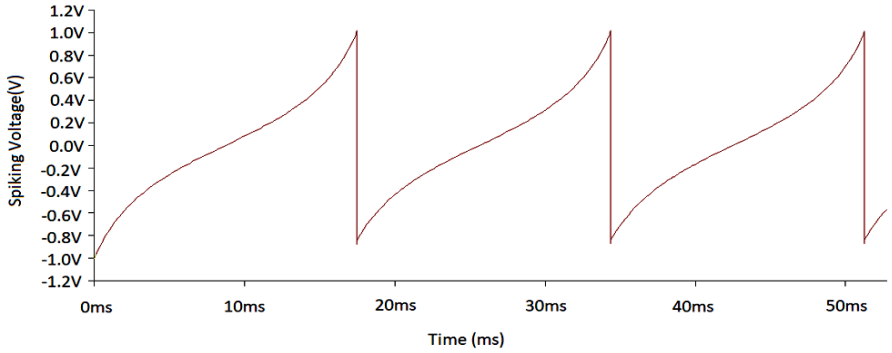

Figure 19. Simulation results for the AQIF CMOS neuron circuit spiking voltage with 58.4 Hz spiking frequency and 17.1 ms spiking period

8. AQIF CMOS NEURON SIMULATION PERFORMANCE

Figure 18 shows the simulation results for the AQIF CMOS neuron circuit quadratic voltage behavior. Figure 19 shows simulation results for the AQIF CMOS neuron circuit spiking voltage and with 58.4 Hz spiking with the V_{peak}=0.95 V and V_{reset}=-0.75 V and a switching threshold of 0.35 V. The tunability of the AQIF CMOS neuron circuit refers to the ability to adjust its parameters to control its behavior characteristics. Figure 19 shows simulation results for the AQIF CMOS neuron circuit spiking voltage with

58.4 Hz spiking frequency and 17.1 ms spiking period. Figure 20 shows simulation results for the AQIF CMOS neuron circuit spiking behavior fast Fourier transform (FFT) with 58.4 Hz spiking frequency. Figure 21 shows simulation results for the AQIF CMOS neuron circuit spiking voltage with 312.5 Hz spiking frequency and 3.2 ms spiking period. Figure 22 shows simulation results for the AQIF CMOS neuron circuit spiking behavior FFT with 312.5 Hz spiking frequency.

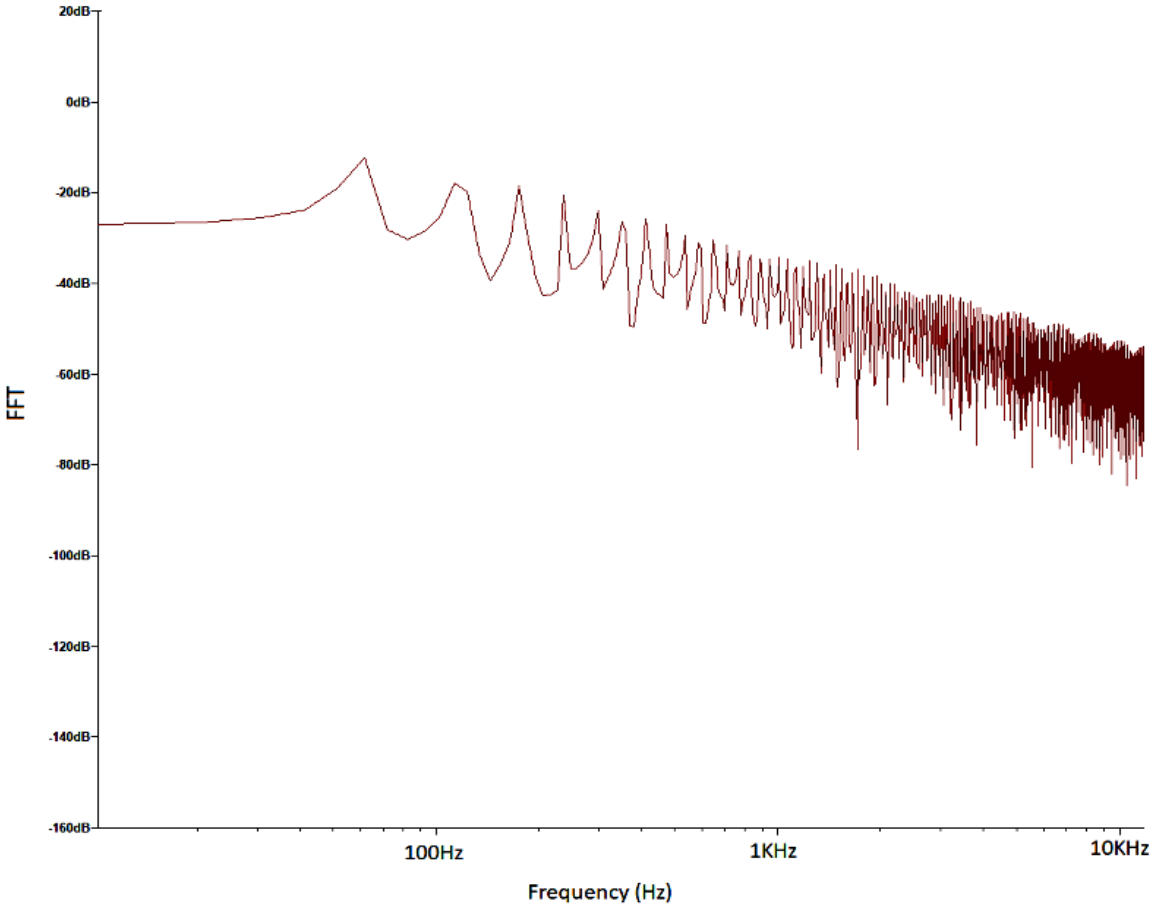

Figure 20. Simulation results for the AQIF CMOS neuron circuit spiking behavior FFT with 58.4 Hz spiking frequency

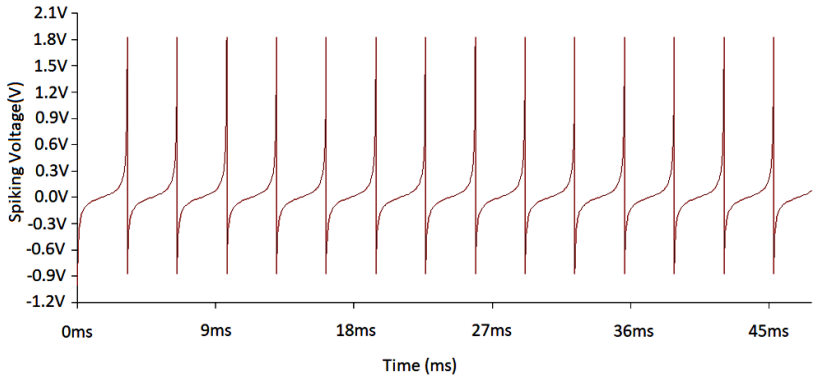

Figure 21. Simulation results for the AQIF CMOS neuron circuit spiking behavior FFT with 312.5 Hz spiking frequency

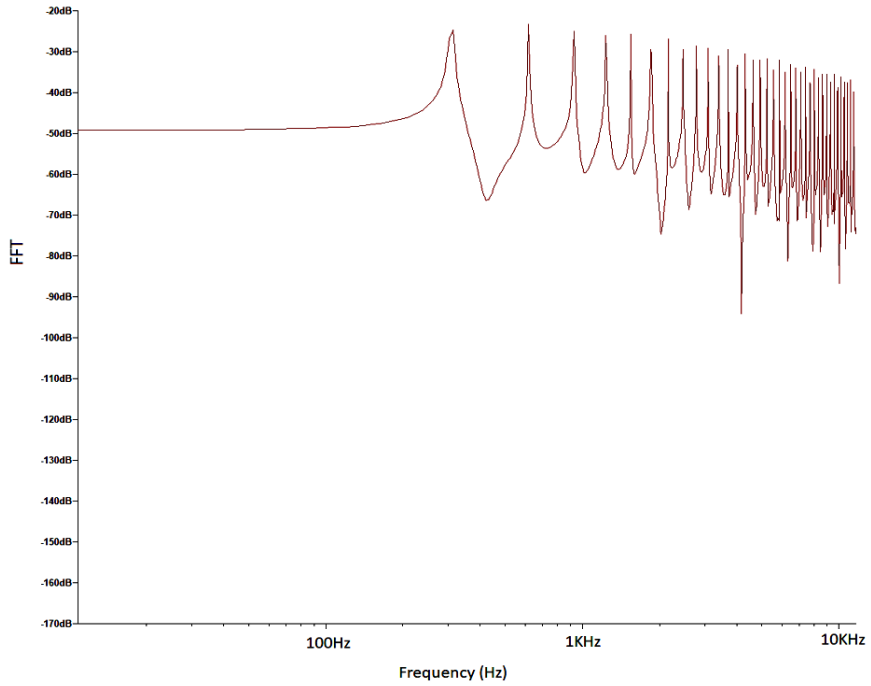

Figure 22. Simulation results for the AQIF CMOS neuron circuit spiking behavior FFT with 312.5 Hz spiking frequency

The fully integrated AQIF CMOS neuron circuit number of transistors is 26 transistors as shown in Table 6. Table 6 shows some of the previously published work was design with less number of transistors. Circuits techniques that may lead to less number of transistors implementation are good to explore in future designs. Fully-integrated CMOS neuron comparison with the AQIF CMOS neuron is shown in Table 7. The tunable spiking frequency CMOS neuron comparison with the proposed AQIF CMOS neuron is shown in Table 7. Tunability is defined as the ability to adjust spiking frequency without changing the input current I. As shown in Table 6, Indiveri and Horiuchi [7] designed his integrate-and-fire neuron with total of 20 transistors and with membrane potential range of 1.5 V in 800 nm CMOS process however it does not have a tuning capability. Indiveri and Horiuchi [7] implemented his integrate-and-fire CMOS neuron using differential pair topology and achieved low power consumption. Srinivasan and Cowan [19] designed his Izhikevich neuron with limited membrane potential range of 150 mV in 65 nm CMOS process with a frequency tuning range of 200 Hz. Srinivasan and Cowan [19] did his CMOS neuron using current-mode circuit topology with total of 18 transistors as shown in Table 5 and with limited tunability capability. Van Schaik *et al.* [34] designed his Izhikevich neuron with total of 17 transistors. Indiveri *et al.* [45] did his QIF neuron with 14 transistors however with no tuning capability. Whereas Ou and Ferreira [36] designed a Morris-Lecar neuron with limited membrane potential range of 200 mV in 180 nm CMOS process with a frequency tuning range of 290 Hz as shown in Table 7.

Table 6. Fully-integrated CMOS neuron comparison with AQIF neuron

	Neuron Model	Transistor Count	Energy/Spike [p]	CMOS Process
Indiveri and Horiuchi [7]	Integrate-and-Fire	20	900	800 nm
Indiveri *et al.* [45]	Quadratic I and F	14	790	350 nm
Srinivasan and Cowan [19]	Izhikevich	18	1060	65 nm
Sourikopoulos *et al.* [33]	Integrate-and-Fire	10	720	65 nm
Van Schaik *et al.* [34]	Izhikevich	17	700	90 nm
This work	AQIF	26	860	130 nm

Table 7. Tunable spiking frequency CMOS neuron comparison with AQIF CMOS neuron

	Configuration	Frequency tuning range	Membrane potential range	Tunability	Process
Indiveri and Horiuchi [7]	Integrate-and-Fire	0 Hz	1.5 V	None	800 nm
Srinivasan and Cowan [19]	Izhikevich	200 Hz	150 mV	Tunable	65 nm
Ou and Ferreira [36]	Morris-Lecar	290 Hz	200 mV	Tunable	180 nm
This Work	Adaptive Quadratic	255 Hz	1.7 V	Tunable	130 nm

9. CONCLUSION

The design of a fully integrated adaptive modified CMOS synapse circuit is presented. By using multiple-gated transistor configuration in the modified CMOS synapse an additional branch provide control where the synaptic output current time-constant is tuned. The effect of changing the multiple-gated transistor bias voltage from 0.25 to 0.45 V tunes the spiking output current exponential time-constant range as shown in simulation results. Our proposed synapse design with multiple-gated transistor configuration achieved a tunable time-constant range of 200 ms compared to previously published work with limited tunable time-constant range to 100 ms. By tuning the decaying exponential time-constant with multiple-gated transistor configuration, the proposed modified CMOS synapse captures the dynamic nature of biological synapses. Moreover, the design of a fully integrated AQIF CMOS neuron was presented as well. A differential pair with variable capacitor integrator and a tunable schmitt trigger threshold detector circuit are integrated in the CMOS neuron that can be tuned varying its spiking frequency. The proposed AQIF CMOS neuron has the ability to adjust the spiking frequency without changing the input current. The simulation results show the proposed AQIF CMOS neuron circuit spiking frequency can be tuned from 58.4 to 312.5 Hz and its spiking period from 17.1 to 3.2 ms with tuning the bias voltage of variable capacitor integrator. Having a peak voltage V_{peak}=0.95 V, a reset voltage V_{reset}=-0.75 V and a voltage threshold of 0.35 V with a membrane potential range of 1.5 V. The proposed CMOS neuron number of transistors is 26 designed in 130 nm process with a supply voltage of 1.8 V and a total power dissipation of 1.8 mW.

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